changing the voltage at one of said row line and said column line to a level sufficient to initiate current flow through said memory element;

discharging the voltage level at the other of said row line and said column line through said memory element and also through a reverse connected diode pair in series with said memory element; and

comparing the voltage on said other of said row line and said column line with a reference voltage to determine a logical state of said memory element.

6. (Amended) The method of claim 2, wherein said act of setting comprises setting said row line and said column line to a voltage level approximately equal to a threshold voltage of said diode plus an additional voltage sufficient to enable a read operation of said memory element.

21. (Amended) A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

setting a plurality of row lines and a plurality of column lines associated with a memory array to a common voltage such that no current flows through said memory element;

changing the voltage at a selected row line to approximately zero volts such that a current flow is initiated from a column line associated with said memory element through

said memory element and through a reverse connected diode pair coupled to said memory element; and

comparing the voltage at said column line with a reference voltage a predetermined time after said act of changing in order to determine a logical state of said memory element.

Cont. A3

24. (Amended) A method of sensing a stored value of a programmable conductor random access memory cell, the method comprising:

setting a column line and a row line associated with said memory cell to a common voltage level; and

reducing said voltage at said row line to a level such that a reverse connected diode pair coupled to a programmable conductor memory element of said cell is activated and such that a voltage potential difference across said memory element is sufficient to read a logical state of said memory element, but insufficient to program said memory element.

27. (Amended) A semiconductor memory structure, comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first side of a reverse connected diode pair, wherein

a second side of said reverse connected diode pair is coupled to said row line;

and

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.

36. (Amended) A processor system, comprising:

a processor; and

a semiconductor memory structure coupled to said processor, said semiconductor memory structure comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first side of a reverse connected diode pair, wherein

a second side of said reverse connected diode pair is coupled to said row line;

and

cont. A4

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.

Add new claims 45-50 as follows.

45. A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

A5

setting a row line and a column line associated with said memory element to respective voltage levels such that no current flows through said memory element;

changing the voltage at one of said row line and said column line to a level sufficient to initiate current flow through said memory element;

discharging the voltage level of the other of said row line and said column line through said memory element and also through a zener diode in series with said memory element; and

comparing the voltage on said other of said row line and said column line with a reference voltage to determine a logical state of said memory element.

46. The method of claim 45, wherein said act of setting comprises setting said row line and said column line to a voltage level approximately equal to a threshold voltage of said zener diode plus an additional voltage sufficient to enable a read operation of said memory element.

47. A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

setting a plurality of row lines and a plurality of column lines associated with a memory array to a common voltage such that no current flows through said memory element; and

changing the voltage of a selected row line to approximately zero volts such that a current flow is initiated from a column line associated with said memory element through said memory element and through a zener diode coupled in series with said memory element.

48. A method of sensing a stored value of a programmable conductor random access memory cell, the method comprising:

setting a column line and a row line associated with said memory cell to a common voltage level; and

reducing said voltage at said row line to a level such that a zener diode coupled to a programmable conductor memory element of said cell is activated and such that a voltage potential difference across said memory element is sufficient to read a logical state of said memory element, but insufficient to program said memory element.

49. A semiconductor memory structure, comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first terminal of a zener diode, wherein

1 diod.

Cont. a5

a second terminal of said zener diode is coupled to said row line; and

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.

50. A processor system, comprising: 1 diode.

a processor; and

a semiconductor memory structure coupled to said processor, said semiconductor memory structure comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first terminal of a zener diode, wherein

Cont. 1
A5

a second terminal of said zener diode is coupled to said row line; and

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.